

DDM 12

3½ Digit LCD Data Display Module

The DDM 12 is a low power 3½ digit data display module which usually operates under microprocessor control. Inputs are CMOS and TTL compatible. Using three inputs; Clock, Data In and Load, it is possible to individually address LCD segments, permitting 0 to 9 and A to F to be displayed plus any other combination of the segments.

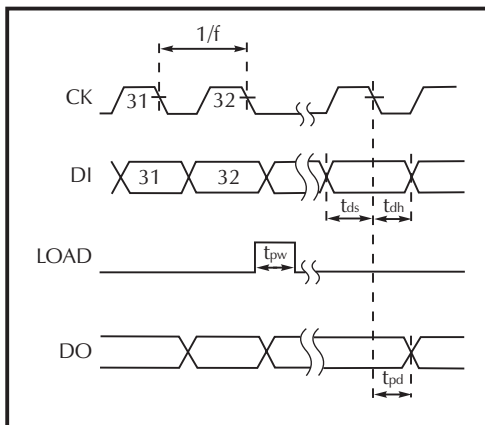
- 🕒 12.5mm (0.5") Digit Height.
- 🕒 Requires Only Three Control Lines
- 🕒 Can be Cascaded
- 🕒 CMOS and TTL Compatible
- 🕒 Easily Interfaced To Microprocessors
- 🕒 5V LED Backlighting
- 🕒 Low Power



Stock Number
Standard Meter

DDM 12

TIMING DIAGRAM



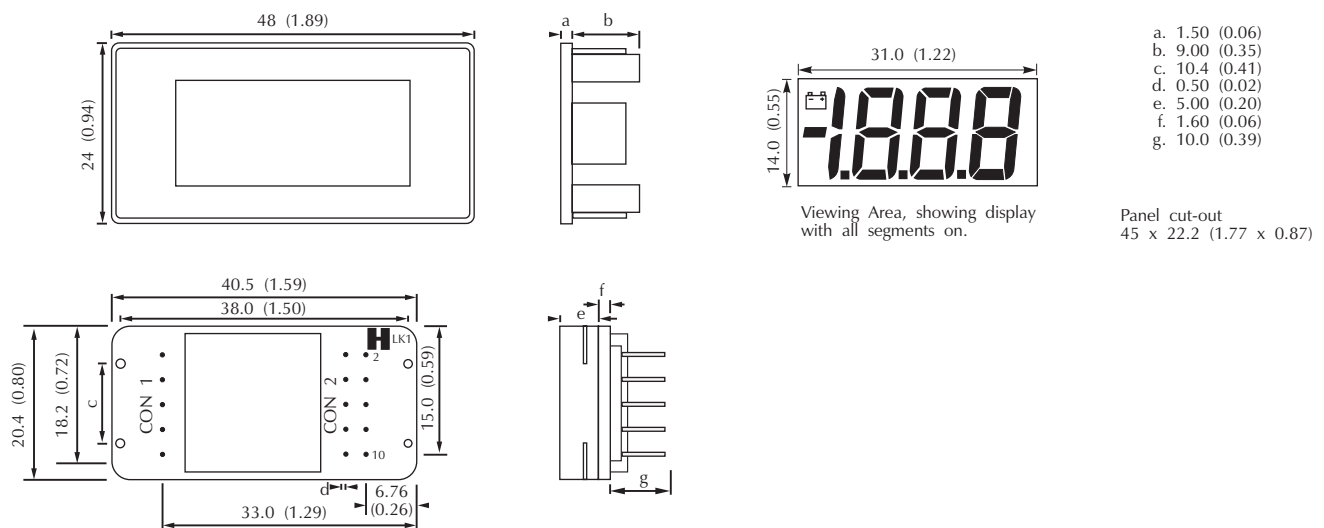
DC CHARACTERISTICS

Specification	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{DD}	3.0	5	8.5	V
Supply current	I _{DD}		40	60	µA
Operating temp. range		0		50	°C
Input High level	V _{IH}	0.5V _{DD}		V _{DD}	V
Input Low level	V _{IL}	0		0.1V _{DD}	V
Input leakage current	I _L		0.01	±10	µA
Input capacitance	C _i			5.0	pF
Backlight voltage	V _{LMP}	4.5	5	5.5	V
Backlight current	I _{LMP}		50	75	mA

AC CHARACTERISTICS

Characteristics	Symbol	Min.	Max.	Units	Conditions
Clock rate	f	0	1.5	MHz	50% duty cycle
Data set-up time	t _{ds}	150		nS	Data change to CK falling edge
Data hold time	t _{dh}	50		nS	CL = 55pF
Load pulse width	t _{pw}	175		nS	
Data out prop. delay	t _{pd}		500	nS	

DIMENSIONS All dimensions in mm (inches)



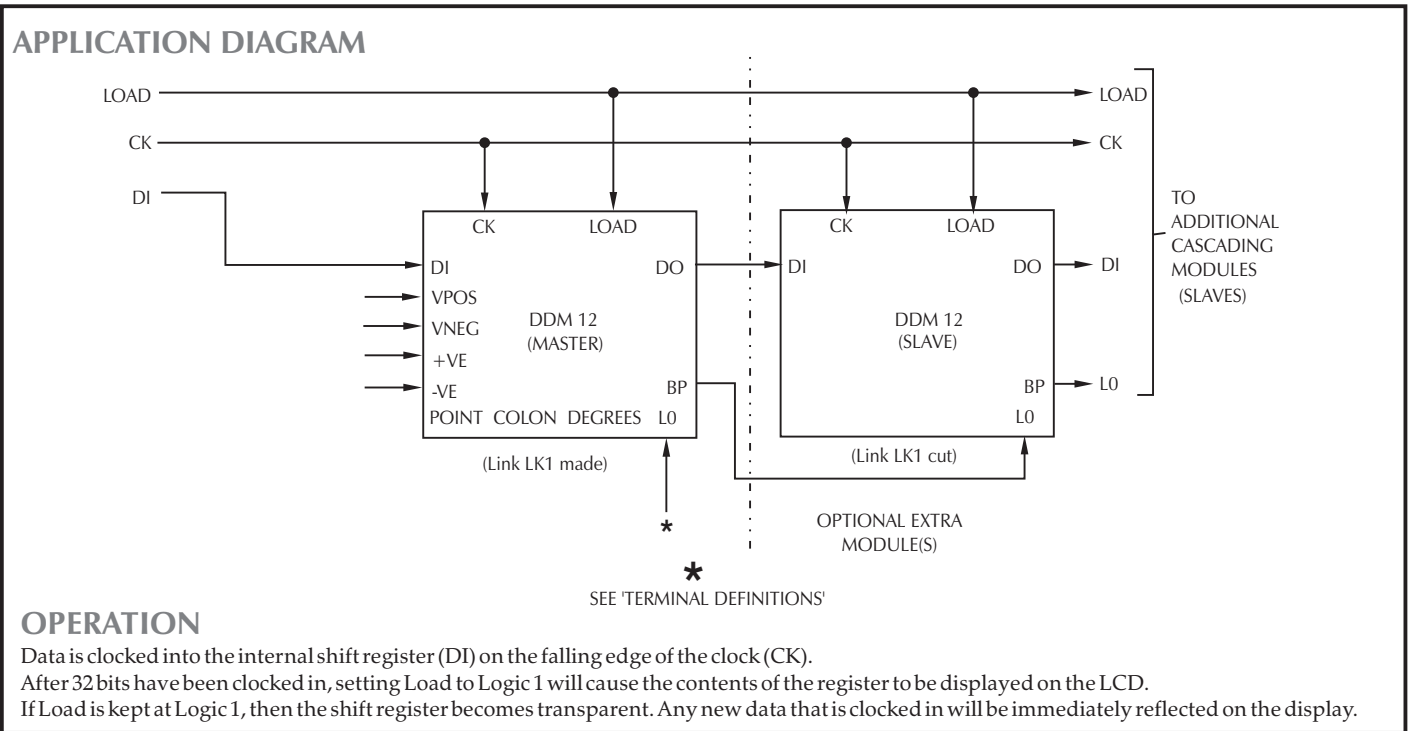
PANEL FITTING

Fit the bezel to the front of the panel and then locate the meter into the bezel from behind. Alternatively the meter and bezel may be assembled before fitting into the front of the panel but care must be taken not to use excessive force. Finally fit the window into the front of the bezel.

PIN FUNCTIONS (CON 2)

- (10) -VE } -5 Volt LED backlighting supply terminals.
- (8) +VE }
- (5) VPOS Positive supply voltage (VDD).
- (1) VNEG Negative supply voltage (VSS).
- (9) LOAD Load input: Causes a parallel load of the data from the shift register to the display latches at logic '1'.
- (7) CK Clock input: The shift register loads, shifts and outputs (DO) on the falling edge.
- (3) DI Data input: A logic '1' on DI causes a segment to be visible.
- (2) DO Data output: To be used for cascading modules.
 For cascading: Connect DO to DI of next module. Each module will produce its own display drive. If an external driving signal is used, connect it to each module's L0 input.
Note: Do not connect backplane outputs together.
- (4) L0 LCD driving signal input. Leave open circuit or use for synchronising cascaded modules (see Application diagram *). When modules are cascaded, slave(s) should have link LK1 cut.
- (6) BP Backplane output.

A 5-way pin header, CON 1, is mounted to add mechanical stability, when plugging the DDM 12 into a PCB. The pins have no electrical function.



DISPLAY SHIFT REGISTER ASSIGNMENT

Note: A segment is visible when a logic '1' is present. For correct operation of the display, 32 bits of data must be clocked in. When clocking in 32 bits of display data the first input bit is the DP of digit 1.



DIGIT	CLOCK PULSE	SEGMENT	DIGIT	CLOCK PULSE	SEGMENT
DIGIT 4 'MSD' (LH digit)	1	n/c	DIGIT 2	17	G
	2	n/c		18	F
	3	n/c		19	A
	4	n/c		20	B
	5	n/c		21	C
	6	LOW BATTERY		22	D
	7	POLARITY		23	E
	8	B & C		24	DP
DIGIT 3	9	G	DIGIT 1 'LSD' (RH digit)	25	G
	10	F		26	F
	11	A		27	A
	12	B		28	B
	13	C		29	C
	14	D		30	D
	15	E		31	E
	16	DP		32	DP